International Journal of Computer Networks and Communications Security

VOL. 3, NO. 3, MARCH 2015, 83–87
Available online at: www.ijcncs.org
E-ISSN 2308-9830 (Online) / ISSN 2410-0595 (Print)

FCA- OE: Fault-Aware and Congestion-Aware Routing Algorithm Based on Odd-Even Algorithm for Network on Chip

Amin Mehranzadeh[1], Mehdi Hoodgar[2] and Faraz Forootan[3]

[1, 2, 3] Department of computer, Dezful Branch, Islamic Azad University, Dezful, Iran

E-mail: [1]mehranzadeh@gmail.com, [2]hoodgar@gmail.com, [3]forootan@gmail.com

ABSTRACT

Routing algorithms play a crucial role in design of the network on chip .Fault and congestion are two situations that effect on the packets latency and energy consumption of NoC. This paper presents a fault and a congestion aware routing algorithm called FCA-OE based on Odd-Even (OE) routing algorithm. The simulation shows the strength of the FCA-OE by comparing it with odd-even routing algorithm under different traffic patterns. The Simulation results prove the FCA-OE routing algorithm can improve the average packet latency and the average packet loss rate (10%) in the presence of permanent faults compared with OE routing algorithm and it is capable to route the packets even with the faulty switches and links in network. Simulation results demonstrate that the FCA-OE routing algorithm provides less average energy consumption as compared to the Fault-Aware Dynamic Routing algorithm.

Keywords: *Network-on-Chip, Routing Algorithm, Adaptive, Fault Aware, Congestion Aware.*

1 INTRODUCTION

The network on chip (NoC) is a layered architecture [1] has been proposed for improve performance and scalability of system on chip (SoC). Figure 1 shows an abstract view of a NOC in this architecture. As shown, each tile consists of a resource (show as R) and a switch or router (show as S). In NoC each resource is connected to the switch by a network interface and each switch is connected to the four neighboring tiles via channels and sending packets via a path consisting of a series of switches and channels [2, 3]. The functioning of network on chip is dependable of effectiveness of the routing algorithms. Routing algorithms choose the best path between source and destination nodes and Communication and performance of the entire system are significantly affected by the routing algorithm [4]. The Routing algorithms, classified into deterministic routing algorithms and adaptive routing algorithms. The deterministic routing algorithms the path selected only by the source and destination nodes. But, in the adaptive routing algorithms, the route taken depends on dynamic network conditions with given a beginning and a destination address. The deterministic routing algorithms because of their simplicity used for routers design and provide low latency when congestion of the network is low. However, the deterministic routing algorithms are likely to suffer from throughput degradation when congestion of the network increases and cannot dynamically responds to network situations. The adaptive routing algorithms by using alternative paths avoid congestion and improve the performance of network on chip. However, the adaptive routing algorithms have a higher latency when congestion of the network is low because of the need to the extra logic in order to choose a better path compared to deterministic routing algorithms [5, 6].

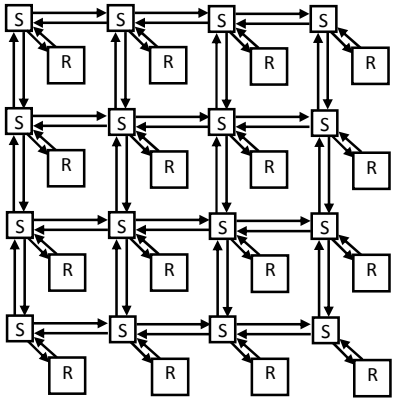

*Fig. 1. The typical structure of a 4*4 NOC*

This paper presents a Fault-aware and congestion-aware routing algorithm called FCA-OE. The proposed routing algorithm can route packets when the network has faulty links or switches. Simulation results demonstrate the advantage of the FCA-OE in terms of packet loss rate and average packet latency as compared to the Odd-Even (OE) routing algorithm when the network has permanent faults. Because of lower average packet latency of the FCA-OE routing algorithm the average packet loss rate is low (less than 10%).

2 RELATED WORKS

The idea of NOC is derived from distributed computing and large scale networks. The routing algorithms for NOC have some tight constraints on memory and computing resources and should be simple and have unique design considerations besides low latency and high throughput [7]. A routing algorithm which is based on Odd-Even routing algorithm and used both deterministic and adaptive routing together is proposed in [3, 8]. In this scheme, when congestion of the network is low the switches work in deterministic mode and work in adaptive mode when congestion of the network increase. For tolerant of the faults, several researches worked on different routing schemes. In order to successful transmission of messages through the network, several copies of the same packet sent along the network links [9]. Similarly, by sending the flood packets to the network as probabilistic flooding algorithms, finally packets reach to the destination [10]. The probabilistic flooding algorithms increase congestion when the network is heavily loaded. In [11], to tolerate the permanent faults, different deterministic routing algorithms have been proposed to avoid of the faulty links. In [12], a fault tolerant routing scheme was suggested to avoid of the faulty links. This paper, introduce a fault and congestion aware dynamic routing scheme for network on chip. The proposed algorithm can locate the faulty links and avoid them in order to prevent packet losses and increase throughput of the network. In addition, the presented algorithm has the advantage of spreading the load over the whole network by using the stress factors.

3 PROPOSED ROUTING ALGORITHM

This paper, present a new fault and congestion aware routing algorithm based on Odd-Even routing, namely fault and congestion aware OE (FCA-OE). Figure 2 shows the pseudo code of the FCA-OE routing algorithm, in FCA-OE a packet routing first according to odd-even routing algorithm and then the best path selected by comparing of the stress factor and the mask (fault mask). The instant packet queue length of input buffer of each router, stress factor, has been employed to pass around the congestion information [14] and the mask is employed in order to prevent packet losses and increase the overall throughput of the network. Our algorithm uses both the stress factor and the acknowledgment signal to reroute the packets around the links with permanent faults and to distribute the network load in order to lessen the probability of congestion [15].

```
FCA-OE Routing Algorithm Source, Destination, SwitchAddress) {

Declare OutPutSet;
  If (Current Switch and Destination are in same Col and Row) {
      Send packet to local & exit;
  } else {
      If (Current Switch and Destination are in same Col) {
            If (Destination Row > Current Switch Row) {
               Add south to OutPutSet;
            } else {
               Add north OutPutSet;
          }} else {
          If (Destination Col > Current Switch Col) {          //Eastbound Messages
             If (Current Switch and Destination are in same Row) {
                Add East to OutPutSet;
             } else {
                If ((Current Switch Col Is Odd) OR (Current Switch Col == Source Col)) {
                   If (Destination Row > Current Switch Row) {
                      Add south to OutPutSet;
                   } else {
                      Add north to OutPutSet;
                   }
                }
                   If ((Destination Col Is Odd) OR ((Destination Col – Current Switch Col) ! =1)) {
                      Add EAST to OutPutSet;
                   }
             }
          } else {          // westbound
             Add West to OutPutSet;
             If (! IsOdd (switchCol)) {
                If (Destination Row > Current Switch Row) {
                   Add south to OutPutSet;
                } else if (Destination and Current Switch is not in same Row) {
                   Add north to OutPutSet;
                }
             }
          }
       }
      }
    //Select a Dimension from OutPutSet to forward the Packet;
    If (there is more than one link) {
       If (All Links are Mask) {
         Output link is -1;
       } else if ((Link1! = Mask) and (Link2==Mask)) {
        Output link is Link1;
       } else if ((Link1 == Mask) and (Link2! =Mask)) {
        Output link is Link2;
       } else if ((Link1! = Mask) and (Link2! =Mask)) {
         if ( Stress of Link1 <= Stress of Link2){
           Output link is Link1;
         } else {
           Output link is Link2;
         }
    }
}
```

Fig. 2. Pseudo code of FCA-OE routing algorithm

4 EXPERIMENTAL RESULTS

A Java based simulator, developed to evaluate the FCA-OE routing algorithm [16]. The simulation is run with OE and FCA-OE routing algorithms and data are collected after a warm-up period of 10000 cycles. The Size of the mesh network is set to be 6×6 tiles and all of input buffers have 5 flits size and use first in first out strategy. The congestion threshold set at 60% of the total buffer's capacity. The performance of each type of routing algorithm is evaluated through average packet loss percent and throughput curves. Throughput defines as follows:

$$\text{Throughput} = \frac{\text{Total received flits}}{\text{Number of nodes} \times \text{Total Cycles}} \quad (1)$$

The performance of each type of routing algorithm is evaluated through average packet loss percent and throughput curves. Where Total received flits refers to the number of whole flits that arrive at their destination, Number of nodes is the number of nodes, and Total cycles is the number of clock cycles between the time of generation of the first message and reception of the last message. Figure 3, shows the throughput under uniform traffic pattern. As shown in Figure 3, FCA-OE routing algorithm performs better than OE under different fault percent schemes. The fault percent is the number of faulty switches in the network that have one link with permanent fault. The packet injection rate is the number of packets injected into the network per cycle (fixed to 150 (packets/cycle)).

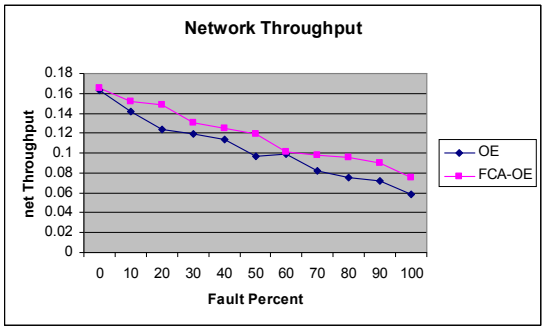

Fig. 3. Network throughput for OE and FCA-OE routing algorithms

Figure 4, shows the average packet received percent under uniform traffic patterns. As shown in this figure, the packet loss rate decreases about 10 percent by FCA-OE.

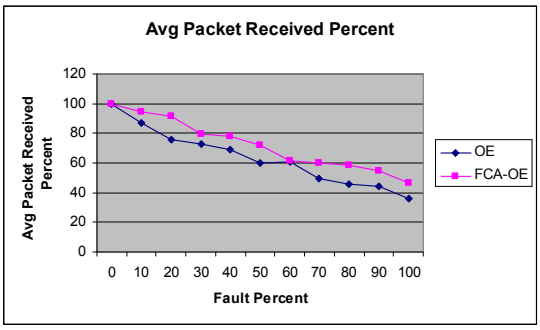

Fig. 4. Average packet received rate under uniform traffic

In order to assess the efficiency of proposed fault and congestion aware dynamic routing algorithm, we carried on a series of experiments to comparing FCA-OE efficiency against the Fault-aware Dynamic Routing algorithm (FADR) [15]. The FADR routing algorithm in terms of functionality, latency, and energy consumption in the presence permanent faults can achieve less latency and provides less energy consumption compared to recently reported fault tolerant routing algorithms such as the flooding algorithms [10]. The performance of the proposed routing algorithm is evaluated through latency-throughput curves [3, 8]. The packet latency is the duration from the time when the first flit is created at the source node, to the time when the last flit is delivered to the destination node. A simulation is conducted to evaluate the average packet latency for a given packet injection rate. For each simulation, latencies are collected after the first 5,000 cycles to allow the network to stabilize and the packet latencies are averaged over 50,000 packets. The packets have a fixed length of 5 flits and the buffer size of input channels is 5 flits.

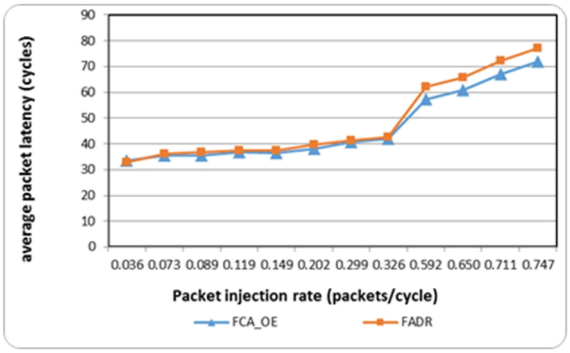

Fig. 5. Average packet latency under uniform traffic when fault percent=0

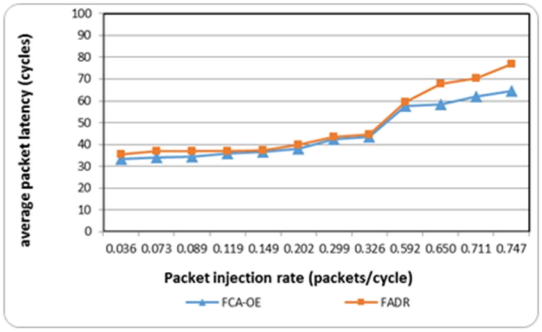

Fig. 5 (b). Average packet latency under uniform traffic when fault percent=10

As shown in Figure 5 (a) and Figure 5 (b), the strength of the FCA-OE routing algorithm is confirmed throughout the experiments by the fact that it achieves shorter average packet latency compared to FADR routing algorithm. The computation of average energy consumption included the number of hops that the flits travel to reach the destination as well as the number of extra flit copies sent through the network because of unacknowledged flits.

As shown in Figure 6, in terms of average energy consumption, the proposed routing algorithm has a consistent behavior in the presence of few faults, which is 1.05× on average less energy consumption compared to the FADR routing algorithm.

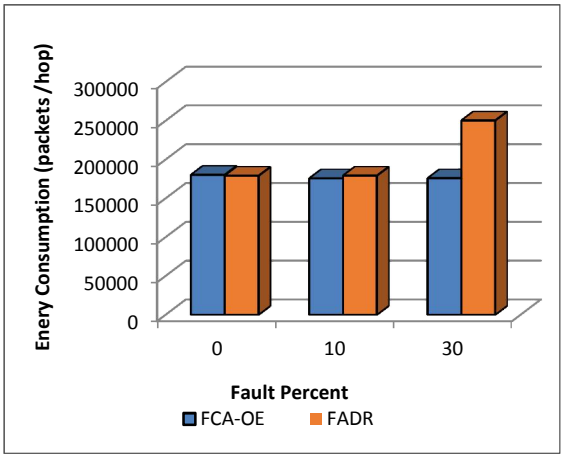

Fig. 6. Average energy consumption for transmitting packets (energy/packet/hop)

5 CONCLUSION & FUTURE WORK

This paper presented a new approach for fault aware and congestion aware routing scheme on the network on chip, namely FCA-OE routing algorithm. The presented routing algorithm distributing the load over the whole network by considering the stress factors. This paper evaluated the result of permanent faults, and packet injection rates on the functioning of the FCA-OE routing algorithm. Simulation results proved the effectiveness of FCA-OE routing algorithm in terms of packet loss percent and latency in the presence of permanent faults compared to odd-even (OE) routing algorithm and proved our algorithm can achieve an average 10 percent less latency and average 10 percent less packet loss rate. The FCA-OE routing algorithm in terms of average energy consumption has less energy consumption as compared to the fault aware Dynamic Routing algorithm (FADR) [15] and recently reported fault tolerant routing algorithms [10].

7 REFERENCES

[1] L. Benini and G.D .Micheli, "Networks on chips: a new SOC paradigm", IEEE Computer, Jan 2002, 35:70–78.

[2] J. Henkel, W. Wolf and S. Chakradhar, "On-chip networks: A scalable, communication-centric embedded system design paradigm", VLSI Design, India, 2004, pp. 845-851.

[3] J. Hu and R. Marculescu, "DyAD - Smart routing for networks-on-chip", DAC, USA, 2004, pp. 260-263.

[4] T. Schonwald, J. Zimmermann, O. Bringmann, "Fully Adaptive Fault-Tolerant Routing Algorithm for Network-on-chip Architectures", 10th Euromicro Conference on Digital System Design Architectures Methods and Tools (DSD), 2007.

[5] W. J. Dally and B. Towles, "Route packets, not wires: On-chip interconnection networks", DAC, USA, 2001, pp. 684-689.

[6] Al. Hashimi, B.M. and Schmitz, "Improving Routing Efficiency for Network-on-Chip through Contention-Aware Input Selection", 11th Conference (ASP-DAC), Japan, 2006.

[7] T. T. Ye, L. Benini, and G. De Micheli, "Packetization and routing analysis of on-chip multiprocessor networks", Journal of Systems Architecture, 2004, vol. 50, pp. 81-104.

[8] G.M. Chiu, "The odd-even turn model for adaptive routing", IEEE Transactions on Parallel and Distributed Systems, 2000, Vol. 11, pp. 729-38.

[9] S. Manolache, P. Eles, and Z. Peng, "Fault and energy-aware communication mapping with guaranteed latency for applications implemented on NOC", in Proceedings of IEEE/ACM Design Automation Conference, DAC, 2005, pp. 266–269.

[10] M. Pirretti, G. Link, R. Brooks, N. Vijaykrishnan, M. Kandemir, and M. Irwin,

"Fault tolerant algorithms for network-on-chip interconnect", in Proceedings of IEEE Computer Society Annual Symposium on VLSI, 2004, pp. 46–51.

[11] D. Greenfield, A. Banerjee, J.G. Lee, and S. Moore, "Implications of rent's rule for NOC design and its fault-tolerance", in Proceedings of International Symposium on Networks-on-Chip, 2007, pp. 283–294.

[12] M. Ali, M. Welzl, and S. Hessler, "A fault tolerant mechanism for handling permanent and transient failures in a network on chip", in Proceedings of International Conference on Information Technology, ITNG, 2007, pp. 1027–1032.

[13] L.M. Ni and P.K. Mckinley, "A survey of wormhole routing techniques in direct networks", IEEE Int, Conference on Computer, Feb. 1993, 26:62-76.

[14] M. Li, Q.A. Zeng, and W.B. Jone, "DyXY - A Proximity Congestion-Aware Deadlock-Free Dynamic Routing Method for Network on Chip", in Proceedings of IEEE/ACM Design Automation Conference, DAC, 2006, pp. 849–852.

[15] A. Hosseini, T. Ragheb, Y. Massoud, "A Fault-Aware Dynamic Routing Algorithm for on-Chip-Networks", IEEE, 2008.

[16] H. Hossain, M. Ahmed, A. Al-Nayeem, "GPNOCSim-A General Purpose Simulator for Network-on-chip", Dhaka, Bangladesh, ICICT, 2007.